

**Serial No.: 09/666,853**

**AMENDMENT TO THE TITLE:**

Please replace the title with the following rewritten title:

INFORMATION PROCESSING DEVICE FOR EXECUTING INSTRUCTIONS FROM AN  
INSTRUCTION STORAGE BY PIPELINE PROCESSING AND DETECTING BRANCHING  
INSTRUCTIONS IN THE INSTRUCTION SEQUENCE

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**AMENDMENTS TO THE DRAWINGS:**

Enclosed herewith are substitute drawings figures 6-8 and 11, labeled "Replacement Figures".

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**REMARKS**

Claims 1-18 are pending in the application. Claims 1-4, 6-9, 14-16, and 18, figures 6-8 and 11, and the title are amended herein. No new matter is added by the amendments, which find support throughout the specification and figures. Reconsideration and allowance of the present application are respectfully requested in light of the amendments and the following remarks.

The Office Action objects to the drawings. New replacement figures for figures 6-8 and 11 are presented herein to respond to the rejection. New replacement figures 6-8 and 11 return the figures to their original form, thereby eliminating the scribble marks objected to by the Examiner. Regarding the objection of the Examiner presented in the Office Action of February 9, 2004, which precipitated the amendments which are objected to in the present Office Action, Applicants submit that the originally filed drawings comply with 37 C.F.R. § 1.81 (b) for drawings required in a patent application, namely, that the drawings include illustrations which facilitate an understanding of the invention (for example, flowsheets in cases of processes, and diagrammatic views). Figures 6-8 and 11 illustrate diagrammatically the present invention, and assist in understanding of the invention, when read in conjunction with the accompanying description in the specification. Therefore, it is respectfully requested that the rejection to the figures therefore be withdrawn.

The Office Action also objects to the title and requests a new title. The title was amended in the preliminary amendment filed on July 9, 2004. It is respectfully submitted that the new title presented therein is sufficiently descriptive, and it is therefore requested that the rejection be withdrawn.

The Office Action objects to the claims, and rejects the claims under 35 U.S.C. § 112, second paragraph, as being indefinite. The claims have been amended to respond to these

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objections and rejections. In particular, claim 16 is amended to remove the reference to "with a pipeline processing". Regarding rejection no. 25, the Examiner states there is no antecedent basis for "the branching instruction inside said first instruction sequence" and "the branching instruction inside said second instruction sequence". However, the instruction (02) of Fig. 2 is defined as "a branching instruction inside said first instruction sequence", and the instruction (04) is defined as "a next branching instruction inside said first instruction sequence". Furthermore, the instruction (12) is defined as "a branching instruction inside said second instruction sequence", and the instruction (14) is defined as "a next branching instruction inside said second instruction sequence". Therefore, applicants respectfully submit that the claims as presented are definite. With respect to the rejection nos. 27 and 28, "said branching instruction" is defined as including both the first and second branching instructions.

It is therefore respectfully requested that the objections and rejections under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claims 1-4, 6-9 and 12 stand rejected under 35 U.S.C. § 102(e) as anticipated by Asato (U.S. 6,289,442). Claim 5 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Asato. Claim 10 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Asato in view of Hara (U.S. 5,740,715). Claim 10 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Asato in view of Shiell (U.S. 5,864,697). Claim 11 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Asato in view of Hara (U.S. 5,740,715). Claims 13-18 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Asato in view of Lee (Lee et al., Instruction Cache Fetch Policies for Speculative Execution, 1995). Applicants respectfully traverse.

Claim 1 is amended to include the feature "without prefetching a branch target instruction sequence of the next branching instruction", and "without prefetching a branch target instruction

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sequence of the second branching instruction". Similarly, claims 2 and 6 are amended to include the similar features.

According to the present invention, as shown in Fig. 2, the first instruction sequence (C1) being processed is stored in one of the instruction buffers (e-1), the second instruction sequence (C2) is prefetched and stored in the other of the instruction buffers (e-2). Further, the first target address information of the next branching instruction (04) is stored in one of the branch target address information buffers (b-1) *without prefetching the branch target instruction sequence (C3) of the next branching instruction (04)*, and the second target address information of the branching instruction (12) is stored in the other of the branch target address information buffers (b-2) *without prefetching the branch target instruction sequence (C4) of the branching instruction (12)*.

The instruction reading request portion does not prefetch the branch target instruction sequences (C3, C4), but waits while holding the first and second target address information in the branch target address information buffers, until the branching instruction is executed. Therefore, the necessary hardware of instruction buffer and target address information buffer can be minimized. Further, branch target instruction prefetching, which may be unnecessary when resulting not branching upon execution, can be avoided before executing the branch instruction.

On the other hand, in Asato, all instruction sequences A1-A8 and B1-B8 are stored in the instruction buffers and only the branch target address information for C1 is stored in the branch target address information buffer without prefetching and storing the branch target instruction sequences C1-C-8. Therefore, Asato does not disclose or suggest all of the features of claims 1, 2, and 6, and therefore claims 1, 2, and 6 are allowable over the reference.

The addition of the secondary references does not cure the critical deficiency discussed

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above in regard to the primary reference. Therefore, since claims 3-5 and 7-11 depend from claims 2 and 6, respectively, these claims are allowable for at least the same reasons as their base claims are allowable.

Claims 12 and 16 include the feature of “wherein, *if a branching direction of said branching instruction is not yet determined*, said cache controller performs a memory bus access to said main memory *according to a branching direction predicted by the branching prediction portion*”. The Office Action cites Asato as disclosing this feature in a section stating:

However, if the branch prediction unit 14 prediction unit 14 predicted the detected branch instruction *as not taken*, then the next block instruction would have been that subsequent to the first branch of instructions in program order (i.e., instructions A9-A16). This feature has the added advantage of combining branch prediction with the technique for tagging and invalidating speculatively issued instructions.

(Asato; col. 13, lines 55-62; emphasis added) . However, the cited section merely refers to the consequences if the branch prediction unit 14 predicts a branch as not taken. The cited section does not appear to address the distinct situation in which the branching direction of the branching instruction is not yet determined, as recited in the claim. Furthermore, the cited section indicates that the next block instruction subsequent to the first branch of instructions is indicated. However, this does not appear to disclose or suggest a cache memory accessing a memory based on the branching direction predicted by the branching prediction portion. Therefore Asato does not disclose all of the features of claim 12. Therefore, the invention of claim 12 is not anticipated by Asato.

The addition of Lee fails to cure the deficiency discussed above in regard to Asato as applied against claim 12, and therefore for at least the same reasons as claim 12 is allowable, claim 16 is also allowable.

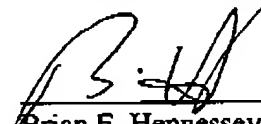
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Since claims 13-15, 17, and 18 depend from claims 12 or 16, respectively, these claims are allowable for at least the same reasons as their respective base claims are allowable.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

  
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Brian E. Hennessey  
Reg. No. 51,271

CUSTOMER NUMBER 026304  
Telephone: (212) 940-6311  
Fax: (212) 940-8986/8987  
Docket No.: FUJH 17.759 (100794-11499)  
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